IN THE CLAIMS

Please amend the claims as follows:

Claims 1-14 (Canceled).

Claim 15 (Currently Amended): An active matrix structure for a display screen, formed on a transparent substrate, comprising:

pixel electrodes arranged in rows and columns;

a switching device associated with each electrode, and corresponding row selection lines, each selection line being disposed between two rows of successive pixel electrodes, said selection lines and electrode pixels being realized on a different level of a structure; ~~and~~

under each row of pixel electrodes, a bus made of conducting and transparent material, substantially with a same width as said row, produced on a level of the structure separated from a level of the selection lines and from a level of the pixel electrodes by at least one insulation layer and connected to the selection line of a previous row of pixel electrodes, said bus forming a storage capacitor with each pixel electrode of said row; and

a channel level of the transistors is situated between a level of the storage capacitor bus and that of the row selection lines forming gate of the transistors.

Claim 16 (Previously Presented): The active matrix structure as claimed in claim 15, wherein each storage capacitor bus is connected to a previous row selection line outside an active zone of the matrix, at at least one end.

Claim 17 (Previously Presented): The active matrix structure as claimed in claim 16, wherein each storage capacitor bus is connected at its two ends to said previous row selection line, outside the active zone.

Claim 18 (Previously Presented): The active matrix structure as claimed in claim 15, wherein each storage capacitor bus is connected to said row selection line at the level of each pixel element of the associated row.

Claim 19 (Previously Presented): The active matrix structure as claimed in claim 15, wherein the switching devices are transistors, the selection line of a row forming a gate for each of the transistors of the row.

Claim 20 (Currently Amended): The active matrix structure as claimed in claim 19, wherein ~~a channel level of the transistors is situated between a level of the storage capacitor bus and that of the row selection lines forming gates of the transistors, and wherein~~ for each transistor of a row, a portion at least of the storage capacitor bus of the following row overlaps the channel of the transistor, said portion of bus operating as a second gate for said transistor.

Claim 21 (Currently Amended): The active matrix structure as claimed in claim 19, wherein ~~a channel level of the transistors is situated between a level of the storage capacitor bus and that of the row selection lines forming gate of the transistors, and wherein~~ for each transistor of a row, a portion at least of the storage capacitor bus of the row overlaps the channel of the transistor, said portion of bus operating as a second gate for said transistor.

Claim 22 (Previously Presented): The active matrix structure as claimed in claim 21, wherein the storage capacitor bus (Rn) of a row (Rn) of rank n in the matrix is connected to a

previous row selection line, the rank of said previous row being determined as a function of a mode of addressing of the display screen in which the matrix must operate.

Claim 23 (Previously Presented): The active matrix structure as claimed in claim 22, wherein for a mode of addressing involving a line inversion, the storage capacitor bus of the row of rank n is connected to the selection line of the row of rank n-2.

Claim 24 (Previously Presented): The active matrix structure as claimed in claim 22, wherein for a mode of addressing involving a double-line inversion, the storage capacitor bus of the row of rank n is connected to the selection line of the row of rank n-4.

Claim 25 (Previously Presented): The active matrix structure as claimed in claim 19, for a transistor of type with a gate below, wherein the storage capacitor bus is produced on a level disposed above the levels of the selection lines and the data lines.

Claim 26 (Previously Presented): The active matrix structure as claimed in claim 19, for a transistor of type with a gate above, wherein the storage capacitor bus is produced on a level disposed below the levels of the selection lines and the data lines, directly on a substrate, or on an optical mask level.

Claim 27 (Previously Presented): A display screen comprising an active matrix structure as claimed in claim 15.

Claim 28 (Previously Presented): The display screen as claimed in claim 27, wherein the switching devices are transistors, the selection line of a row forming gate for each of the

transistors of the row, and wherein the row selection lines are driven by a line addressing signal of a pulse type having plural voltage levels.

Claim 29 (Previously Presented): The active matrix structure as claimed in claim 20, for a transistor of type with a gate below, wherein the storage capacitor bus is produced on a level disposed above the levels of the selection lines and the data lines.

Claim 30 (Previously Presented): The active matrix structure as claimed in claim 20, for a transistor of type with a gate above, wherein the storage capacitor bus is produced on a level disposed below the levels of the selection lines and the data lines, directly on a substrate, or on an optical mask level.

Claim 31 (Previously Presented): A display screen comprising an active matrix structure as claimed in claim 29.

Claim 32 (Previously Presented): A display screen comprising an active matrix structure as claimed in claim 30.